Sub A6

Abstract of the Disclosure

A pipelined multistreaming processor has an instruction source, a plurality of streams fetching instructions from the instruction source, a dispatch stage for selecting and dispatching instructions to a set of execution units, a set of instruction queues having one queue associated with each stream in the plurality of streams, and located in the pipeline between the instruction cache and the dispatch stage, and a select system for selecting streams in each cycle to fetch instructions from the instruction cache. The processor is characterized in that the select system selects one or more streams in each cycle for which to fetch instructions from the instruction cache, and in that the number of streams selected for which to fetch instructions in each cycle is fewer than the number of streams in the plurality of streams.